## Lab 4

## Required lab tools: Logisim

## [Step 1: 1-bit Addition]

1. Create a new Logisim Circuit by clicking "Project" -> "Add Circuit". Name this circuit "1-bit Full Adder".
2. Implement the following truth table by first converting this table into a boolean algebraic expression and then creating the circuits. You are not required to minimize the boolean algebraic expression, although it may help in designing your circuit.

| A | B | Cin | Sum (output) | Cout (output) |
| :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

3. Test your circuit to make sure that it properly implements full addition.

## [Step 2: Combining 1-bit adders]

1. Go back to the main circuit by double clicking "main" in the toolbox:

| 4-bit adder |  |
| :---: | :---: |
|  | main |
|  | 1-bit full adder |
| (- | Wiring |
| (- | Gates |
| $\pm$ | Plexers |
| ¢- | Arithmetic |
| + | Memory |
| †- | Input/Output |
| ¢ | Base |

Now single click on the 1-bit full adder and notice that you can create several 1-bit adders using the circuity that you just developed:
2. You will need four of these 1-bit full adders to make a 4-bit full adder.
3. Create two 4-bit input pins ( $A$ and $B$ ) by selecting the data width in the options toolbox:

| Facing | East |
| :--- | :--- |
| Output? | No |
| Data Bits | 4 |
| Three-state? | No |
| Pull Behavior | Unchanged |
| Label | B |
| Label Location | West |
| Label Font | SansSerif Plain 12 |

4. Do the same for a 4-bit output labeled $S$ (sum).
5. You will also need a 1-bit output pin labeled Cout (carry out).
6. To split the data from 4 bits to single bits, you need to use a splitter:

|  |  |
| :--- | :--- |
|  |  |
| Selection: Splitter |  |
| Facing | East |
| Fan Out | 4 |
| Bit Width In | 4 |
| Appearance | Centered |
| Bit 0 | 0 (Top) |
| Bit 1 | 1 |
| Bit 2 | 2 |
| Bit 3 | 3 (Bottom) |
|  |  |

7. Link the four bit adders' carry bits together:

8. Notice how the carry out of the first adder is linked to the carry in the second adder. This is known as "rippling" the carry from one adder to the other. Notice how the last adder links to the Carry Out output pin.

## [Step 3: Putting It Together]

1. Split the four-bit A input among the four 1-bit adders (top pin)
2. Combine the four one-bit adders' output to another splitter connected to the output pin $S$ (sum):

3. Using the finger tool, change the inputs of $A$ and $B$ to see what you get for Sum and Cout. Make sure that it conforms to the boolean algebraic expressions:

$$
\begin{aligned}
& \text { Sum }=\overline{A B C}+\bar{A} B \bar{C}+A \overline{B C}+A B C \\
& \text { Cout }=\bar{A} B C+A \bar{B} C+A B \bar{C}+A B C
\end{aligned}
$$




As you can see with this example, 0110 [6] + 0111 [7] = 1101 [13] (Carry 0)

## [Step 4: Two's Complement]

1. Allow for subtraction by creating a two's complement on the $B$ input pin. You will need to create another 1bit input pin called "Subtraction" that when flipped to $1, B$ is given the twos complement.
2. You can do two's complement by adding XOR gates for each of B's input bits. The "Subtraction" bit needs to be connected to the second input pin on each of the XOR gates.
3. Finally, connect the "Subtraction" bit to the carry-in bit of the first 1-bit adder. This will add 1 to the sum (remember two's complement is complement +1 ).
4. This effectively takes the twos' complement of the $B$ input and adds them together.

Save your logisim circuit by exporting a PNG image. Attach this in your submission along with your original .png files! You should have lab4.circ and lab4a.png, lab4b.png and then lab4c.circ and lab4c.png.

## [You are finished with this lab!]

Export your 1-bit, 4-bit, and two's complement circuits as lab4a.png, lab4b.png, and lab4c.png. Attach these three pictures as your submission along with your circuit file. You should have lab4.circ and lab4a.png, lab4b.png, and lab4c.png.

Points 100

Submitting a file upload

File Types png and circ

| Due | For | Available from | Until |
| :--- | :--- | :--- | :--- |
| Sep 19, 2017 | Everyone | Sep 15, 2017 at 7:58am | Sep 19, 2017 at 11:59pm |

## Lab 4




